UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,282	11/20/2003	Koji Tanonaka	02-51786	3194

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EXAMINER
NAJEE-ULLAH, TARIQ S

ART UNIT	PAPER NUMBER
2453	

NOTIFICATION DATE	DELIVERY MODE
09/30/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _06 August 2010_.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-9_ is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) _1-9_ is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All   b)☒ Some * c)☐ None of:
   1.☒ Certified copies of the priority documents have been received.
   2.☐ Certified copies of the priority documents have been received in Application No. _____.
   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).
   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August

6, 2010 has been entered.

Response to Amendment

2.   This Office action has been issued in response to Applicant's Amendment filed

August 6, 2010. Claims 1-9 are pending in the case. No claims have been canceled or

added. Claims 1 and 4 have been amended.

Response to Arguments

3.   The rejections to claims 4-9 rejected under 35 U.S.C. 101 have been withdrawn

in light of this amendment.

        Applicant's arguments with respect to claims 1-9 rejected under 35 U.S.C. 103(a)

as being unpatentable over US Patent 6,618,455 to Maeda et al (Maeda hereinafter) in

view of US 2004/0208568 to Sweeney et al (Sweeney hereinafter) and further in view of

US 2004/0156325 to Perkins et al (Perkins hereinafter) have been considered but are

not found persuasive. Applicant argues that Maeda-Sweeney-Perkins fails to teach or

suggest "*a PLL circuit to receive one of the clock signals and generate another clock

signal in sync with the received one of the clock signals wherein the first synchronous*

state indication code is converted into the second synchronous state indication code by use of a conversion table." Examiner respectfully disagrees. Maeda-Sweeney-Perkins clearly teaches **and a PLL circuit** (Maeda, col. 4, lines 45-61) **to receive one of the clock signals and generate another clock signal in sync with the received one of the clock signals** (Maeda, col. 4, lines 45-61) **wherein the first synchronous state indication code is converted into the second synchronous state indication code** (Sweeney, ¶ 27, 43, 62; fig. 2) **by use of a conversion table** (Maeda, col. 3, lines 14-21). Examiner maintains previous rejection.

Priority

4.   Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a certified English translation of the foreign application must be submitted in reply to this action. 37 CFR 41.154(b) and 41.202(e).

Failure to provide a certified translation may result in no benefit being accorded for the non-English application.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,618,455 to Maeda et al (Maeda hereinafter) in view of US 2004/0208568 to

Sweeney et al (Sweeney hereinafter) and further in view of US 2004/0156325 to

Perkins et al (Perkins hereinafter).

Regarding claims 1 and 4, Maeda teaches **a synchronous network**

establishing method of establishing a synchronous network in which a node

apparatus conforming to a first synchronization scheme and a node apparatus

conforming to a second synchronization scheme co-reside (Maeda, col. 1, line 60 –

col. 2, line 16). Maeda does not explicitly teach **wherein the first synchronization**

scheme and the second synchronization scheme implement different

synchronous state indication codes for establishing the synchronous network,

said method comprising: receiving a first state indication code used by the first

synchronization scheme to indicate a state of a clock signal with respect to each

of a plurality of clock signals employed in the first synchronization scheme;

converting the first synchronous state indication code used by the first

synchronization scheme into a second synchronous state indication code used

by the second synchronization scheme when the node apparatus conforming to

the second synchronization scheme receives the first synchronous state

indication code from the node apparatus conforming to the first synchronization

scheme, the second synchronous state indication code being used by the second

synchronization scheme to indicate a state of a clock signal with respect to each

of the plurality of clock signals employed in the second synchronization scheme,

wherein the first synchronous state indication code is converted into the second

synchronous state indication code such that plural values of the first

synchronous state indication code different from each other are assigned to

respective values of the second synchronous state indication code different from

each other.

Sweeney teaches **wherein the first synchronization scheme and the second**

synchronization scheme implement different synchronous state indication codes

for establishing the synchronous network (Sweeney, ¶ 27, 43; fig. 2), **said method**

comprising: receiving a first state indication code used by the first

synchronization scheme to indicate a state of a clock signal with respect to each

of a plurality of clock signals employed in the first synchronization scheme

(Sweeney, ¶ 27, 43, 62; fig. 2)**; converting the first synchronous state indication**

code used by the first synchronization scheme into a second synchronous state

indication code used by the second synchronization (Sweeney, ¶ 27, 43, 62; fig. 2)

scheme when the node apparatus conforming to the second synchronization

scheme receives the first synchronous state indication code from the node

apparatus conforming to the first synchronization scheme (Sweeney, ¶ 27, 43, 62;

fig. 2)**, the second synchronous state indication code being used by the second**

synchronization scheme to indicate a state of a clock signal (Sweeney, ¶ 27, 43,

62; fig. 2)**with respect to each of the plurality of clock signals employed in the**

second synchronization scheme(Sweeney, ¶ 27, 43, 62; fig. 2)**; and a PLL circuit**

(Maeda, col. 4, lines 45-61) **to receive one of the clock signals and generate**

another clock signal in sync with the received one of the clock signals (Maeda,

col. 4, lines 45-61) **wherein the first synchronous state indication code is**

converted into the second synchronous state indication code (Sweeney, ¶ 27, 43,

62; fig. 2) **by use of a conversion table** (Maeda, col. 3, lines 14-21).

To provide the method of Maeda with additional functionality of converting the

SDH to SONET or vice-versa would have been obvious to one of ordinary skill in the art,

in view of the teachings of Sweeney, since all the claimed elements were known in the

prior art and one skilled in the art could have combined the elements as claimed by

known methods with no change in their respective functions, and the combination would

have yielded nothing more than predictable results to one of ordinary skill in the art at

the time of the invention.

Maeda-Sweeney fails to explicitly teach **such that plural values of the first**

synchronous state indication code different from each other are assigned to

respective values of the second synchronous state indication code different from

each other.

Perkins teaches **such that plural values of the first synchronous state**

indication code different from each other are assigned to respective values of the

second synchronous state indication code different from each other (Perkins, fig.

3,4,5; ¶ 7, 16, 45). To provide the method of Maeda-Sweeney with additional

functionality of mapping the differing SDH to differing SONET codes or vice-versa would

have been obvious to one of ordinary skill in the art, in view of the teachings of Perkins,

since all the claimed elements were known in the prior art and one skilled in the art

could have combined the elements as claimed by known methods with no change in

their respective functions, and the combination would have yielded nothing more than predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 2, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 1 above including, **further comprising including the first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme and the second scheme in an empty bit** (Maeda, fig. 2, col. 5, line 37-56) **of the converted second synchronous state indication code** (Sweeney, ¶ 27, 43; fig. 2).

Regarding claim 3, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 1 above including, **further comprising using a pre-converted synchronous state indication code included in an empty bit** (Maeda, fig. 2, col. 5, line 37-56) **of the first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme and the second scheme** (Sweeney, ¶ 27, 43, 62; fig. 2).

Regarding claim 5, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 4 above including, **further comprising: a selecting unit to select one of the synchronous state indication code supplied from the counterpart node apparatus** (Maeda, fig. 16, col. 4, line 27-61) **and the converted synchronous state indication code obtained by the synchronous state indication code converting unit** (Sweeney, ¶ 27, 43; fig. 2).

Regarding claim 6, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 5 above including, **wherein the selecting unit administers**

switching according to a switching instruction signal (Maeda, clock switching unit, col. 1, line 66 – col. 2, line 35).

Regarding claim 7, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 5 above including, **further comprising: a switch unit to instruct a switching of the selecting unit** (Maeda, clock switching unit, col. 1, line 66 – col. 2, line 35).

Regarding claim 8, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 5 above including, **further comprising: a switching instruction unit to detect a bit of a signal supplied from the counterpart node apparatus to determine which of the first scheme and the second scheme said counterpart node apparatus conforms to, and to instruct a switching of the selecting unit based on the determination** (Maeda, clock switching unit, col. 1, line 66 – col. 2, line 61).

Regarding claim 9, Maeda-Sweeney-Perkins discloses the invention substantially as described in claim 4 above including, **wherein a content to be converted by the synchronous state indication code converting unit can be arbitrarily changed** (Maeda, clock switching unit, col. 1, line 66 – col. 2, line 61).

Conclusion

9.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to TARIQ S. NAJEE-ULLAH whose telephone number is (571)270-5013. The examiner can normally be reached on Monday through Thursday 8:00 - 6:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Joseph Thomas can be reached on (571) 272-6776. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. S. N./
Examiner, Art Unit 2453
September 15, 2010

/Philip J Chea/
Primary Examiner, Art Unit 2453